

Application No. 09/767,149  
Amdt. dated August 12, 2004  
Reply to Office Action of April 14, 2004  
Docket No. 8027-1027

**APPENDIX:**

The Appendix includes the following item:

- copy of an English translation of KANEDA JP 11-271715.

**\* NOTICES \***

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**CLAIMS**

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**[Claim(s)]**

[Claim 1] Two or more pixel electrodes arranged in the shape of a matrix, and two or more signal lines and scanning lines which are wired by said pixel electrode through a thin film transistor. The liquid crystal display panel containing the liquid crystal layer arranged between the counterelectrode which counters said pixel electrode, and said pixel electrode and said counterelectrode. The signal-line drive circuit connected to said signal line, and the scanning-line drive circuit connected to said scanning line. In the active matrix liquid crystal display which displays based on the control signal and data signal which equip said counterelectrode with the counterelectrode drive circuit which supplies an opposite electrical potential difference, and the detector which detects abnormalities of operation or termination, and are supplied from the outside Said scanning-line drive circuit is an active matrix liquid crystal display characterized by accomplishing said thin film transistor connected to said all scanning lines based on the output of said detector with switch-on.

[Claim 2] Said signal-line drive circuit is an active matrix liquid crystal display according to claim 1 characterized by outputting said counterelectrode electrical potential difference based on the output of said detector.

[Claim 3] Said signal-line drive circuit is an active matrix liquid crystal display according to claim 2 characterized by including the switchable change-over circuit section for the reference voltage of said pair in said counterelectrode electrical potential difference based on the output of said detector including the digital-to-analog transducer containing the resistance elements by which the series connection was carried out between the reference voltages of a pair.

[Claim 4] Said detector is an active matrix liquid crystal display according to claim 1 characterized by inspecting said control signal.

[Claim 5] Two or more pixel electrodes arranged in the shape of a matrix, and two or more signal lines and scanning lines which are wired by said pixel electrode through a thin film transistor. The liquid crystal display panel containing the liquid crystal layer arranged between the counterelectrode which counters said pixel electrode, and said pixel electrode and said counterelectrode. The signal-line drive circuit connected to said signal line, and the scanning-line drive circuit connected to said scanning line. In the active matrix liquid crystal display which displays based on the control signal and data signal which equip said counterelectrode with the counterelectrode drive circuit which supplies an opposite electrical potential difference, and the detector which detects abnormalities of operation or termination, and are supplied from the outside Said signal-line drive circuit is an active matrix liquid crystal display characterized by outputting said counterelectrode electrical potential difference to said all signal lines based on the output of said detector.

[Claim 6] Said detector is an active matrix liquid crystal display according to claim 5 characterized by inspecting said control signal.

[Claim 7] Said signal-line drive circuit is an active matrix liquid crystal display according to claim 5 characterized by including the switchable change-over circuit section for the reference voltage of said pair in said counterelectrode electrical potential difference based on the output of said detector including the digital-to-analog transducer containing the resistance elements by which

the series connection was carried out between the reference voltages of a pair.

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[Translation done.]

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the drive circuitry of the active matrix liquid crystal display which was applied to the liquid crystal display, especially was equipped with the switching device for every display pixel.

[0002]

[Description of the Prior Art] In recent years, a thin shape and since it is a low power in addition lightweight, a liquid crystal display has come to be used in various fields. Since the active matrix liquid crystal display with which the switching device was prepared for every display pixel especially can hold down a cross talk to min between contiguity pixels, it is used in the field as which a high definition display image is required especially.

[0003] For example, between an array substrate and an opposite substrate, twist nematic (TN) mold liquid crystal is held through the orientation film, and this active matrix liquid crystal indicating equipment changes.

[0004] Two or more signal lines and two or more scanning lines are mutually wired in the shape of a matrix through an insulator layer, a pixel electrode is arranged through switching devices, such as a thin film transistor (TFT), as a switching device near [ intersection ] each, and an array substrate changes. Moreover, an opposite substrate contains the counterelectrode which counters a pixel electrode.

[0005] In such a liquid crystal display, if direct current voltage continues being impressed to a liquid crystal layer over a long period of time, ion components, such as an impurity [ \*\*\* / in a liquid crystal layer / un- ], will concentrate on one electrode side, and will promote degradation of a liquid crystal layer. For this reason, in the liquid crystal display, making the directions of the inter-electrode potential difference of a pair differ for every 1 vertical-scanning period, and usually driving is performed.

[0006]

[Problem(s) to be Solved by the Invention] By the way, in the liquid crystal display mentioned above, after making mutually the electrical potential difference of a signal line, and the electrical potential difference of a counterelectrode into a grand level at the time of display termination or the abnormal termination at the time of a clock halt etc. in order to prevent degradation of a liquid crystal layer, turning off a power source is proposed. However, if it is in such a configuration, since it is in the condition that the charge was still held at the liquid crystal capacity  $C_{lc}$  or the auxiliary capacity  $C_s$  and direct current voltage will continue being impressed to a liquid crystal layer also after a power source OFF for this reason, it has fully come to prevent degradation of a liquid crystal layer.

[0007] Moreover, as described above, in order to set the electrical potential difference of a signal line, and the electrical potential difference of a counterelectrode as a grand level, respectively, control of each drive circuit system is needed, and there is fault that a configuration is complicated.

[0008] This invention coped with the above-mentioned technical technical problem, was accomplished, and aims at offering the active matrix liquid crystal display which can secure good

display grace over the long period of time by comparatively easy circuitry.

[0009]

[Means for Solving the Problem] Two or more pixel electrodes with which invention indicated by claim 1 is arranged in the shape of a matrix. Two or more signal lines and scanning lines which are wired by the pixel electrode through a thin film transistor. The liquid crystal display panel containing the liquid crystal layer arranged between the counterelectrode which counters a pixel electrode, and a pixel electrode and a counterelectrode. The signal-line drive circuit connected to a signal line, and the scanning-line drive circuit connected to the scanning line. In the active matrix liquid crystal display which displays based on the control signal and data signal which equip a counterelectrode with the counterelectrode drive circuit which supplies an opposite electrical potential difference, and the detector which detects abnormalities of operation or termination, and are supplied from the outside A scanning-line drive circuit is shown in the active matrix liquid crystal display characterized by accomplishing the thin film transistor connected to all the scanning lines based on the output of a detector with switch-on.

[0010] Moreover, two or more pixel electrodes with which invention according to claim 5 is arranged in the shape of a matrix. Two or more signal lines and scanning lines which are wired by the pixel electrode through a thin film transistor. The liquid crystal display panel containing the liquid crystal layer arranged between the counterelectrode which counters a pixel electrode, and a pixel electrode and said counterelectrode. The signal-line drive circuit connected to a signal line, and the scanning-line drive circuit connected to the scanning line. In the active matrix liquid crystal display which displays based on the control signal and data signal which equip a counterelectrode with the counterelectrode drive circuit which supplies an opposite electrical potential difference, and the detector which detects abnormalities of operation or termination, and are supplied from the outside A signal-line drive circuit outputs a counterelectrode electrical potential difference to all signal lines based on the output of said detector.

[0011] According to the above-mentioned configuration, by comparatively easy circuitry, the direct current voltage [\*\*\*\* / un-] impressed to a liquid crystal layer at the time of termination of operation or abnormality actuation can be removed, and display grace with a good rear spring supporter can be secured to this at the long period of time of \*\*.

[0012]

[Embodiment of the Invention] Hereafter, the active matrix liquid crystal display of one example of this invention is explained to a detail with reference to a drawing. This liquid crystal display 1 is the liquid crystal panel 3 of the light transmission mold which is a active-matrix mold with the effective viewing area 5 of 12.1 inches of vertical angles, and an XGA specification, and is displayed using the light source light from a back light 7 as it is a display for (personal computers PC) and is shown in drawing 1 . It contains.

[0013] Although this liquid crystal panel 3 is not illustrated between the array substrate 11 and the opposite substrate 41, twist nematic (TN) mold liquid crystal with a thickness of about 5 microns is held through the orientation film, a polarizing plate is stuck and it is constituted by the outside surface, respectively.

[0014] The array substrate 11 is the scanning line Yj (j=1, 2, ..., 768) which consists of 768 molybdenum tungsten (MoW) alloys arranged on a glass substrate. The signal line Xi (i= 1, 2, ..., 1024x3) which consists of 1024x3 aluminum which intersects perpendicularly through the silicon nitride film (SiNx) which serves as the gate dielectric film 13 of TFT21 mentioned later is included. And near the intersection of the scanning line Yj and a signal line Xi, TFT21 of the gate electrode 15 drawn from the scanning line Yj, the drain electrode 18 drawn from the signal line Xi, and the reverse stagger structure equipped with the amorphous silicon (a-Si) film as a barrier layer is arranged. This source electrode 19 of TFT21 is electrically connected to the pixel electrode 25 which consists of a transparent electrode. Laminating arrangement of this pixel electrode 25 is carried out through the silicon nitride film (SiNx) which serves as gate dielectric film to the scanning line Yj of the preceding paragraph, and the auxiliary capacity Cs is formed between the pixel electrode 25 and scanning-line Yj-1 of the preceding paragraph. In addition, it is not necessary to carry out direct laminating arrangement of the scanning line Yj and the pixel electrode 25 for example, it connects with other metallic materials electrically, and you may

make it superimpose this auxiliary capacity  $C_s$  mutually. For example, the electrode which counters the scanning line  $Y_j$  at the same process as signal-line  $X_i$  formation may be formed in the pixel electrode 25.

[0015] In this example, the alloy of aluminum, aluminum, and rare earth elements, copper, or its alloy is [ other than a molybdenum tungsten (MoW) alloy ] usable as low electrical resistance materials as the scanning line  $Y_j$ .

[0016] Although the opposite substrate 41 is not illustrated on a glass substrate, between a glass substrate 40 and a counterelectrode, a light-shielding film, a color filter, etc. are arranged including the counterelectrode which consists of a transparent electrode.

[0017] Each of the signal line  $X_i$  of this liquid crystal panel 3 is pulled out at the end side of the array substrate 11, and each of the scanning line  $Y_j$  is also pulled out in the signal-line drive circuit 71 which supplies the video-signal electrical potential difference  $V_{Xi}$  to a signal line  $X_i$ , respectively at other end side of the array substrate 11, and it is connected to the scanning-line drive circuit 81 which supplies the scan pulse  $VY_j$ . Moreover, the counterelectrode 43 (refer to drawing 2 ) of a liquid crystal panel 3 is connected to the electrical-potential-difference conversion means 61 which serves as a counterelectrode drive circuit.

[0018] The signal-line drive circuit 71 and the scanning-line drive circuit 81 operate based on an electrical-potential-difference conversion means 61 to change into a predetermined electrical potential difference the reference voltage  $V_{ref}$  of 3V which are controlled by the liquid crystal controller 51 shown in drawing 2 , respectively, and are supplied from PC.

[0019] The liquid crystal controller 51 includes the supervisory circuit 53 which supervises reference clock CK which generates the level clock signal CPH, level start signal STH, the perpendicular clock signal CPV, the perpendicular start signal STV, etc., and is supplied from the PC side based on synchronizing signal H/Vsync and the reference clock signal CK which are supplied from the PC side, as shown in drawing 2 . The liquid crystal controller 51 supervises the existence of the reference clock signal CK by the supervisory circuit 53, and when the reference clock signal CK is not normal, it outputs the 3rd control signal CONT3 of a low level after the 1st and 2nd high-level control signals CONT1 and CONT2 and predetermined period progress.

[0020] The electrical-potential-difference conversion means 61 supplies two kinds of electrical potential differences  $V_{ref1}$  and  $V_{ref2}$  for digital to analog conversion to the signal-line drive circuit 71, and supplies the electrical potential difference  $V_{gon}$  corresponding to the high level of the scan pulse  $VY_j$ , and the electrical potential difference  $V_{goff}$  corresponding to a low level to the scanning-line drive circuit 81, respectively. Moreover, the electrical-potential-difference conversion means 61 supplies the counterelectrode electrical potential difference  $V_{com}$  to a counterelectrode 43 and the signal-line drive circuit 71, respectively. And it is constituted so that supply of the various above-mentioned electrical potential differences may be suspended corresponding to the 3rd control signal CONT3 from the liquid crystal controller 51.

[0021] Next, the signal-line drive circuit 71 is explained with reference to drawing 2 thru/or 3. This signal-line drive circuit 71 receives the level clock signal CPH and level start signal STH from the liquid crystal controller 51, and a shift register 72 carries out the sequential transfer output of level start signal STH based on the level clock signal CPH. It is based on an output from this shift register 72, and is digital - Analog - A conversion circuit (DAC) 73 changes digital image data DAT A into the video-signal electrical potential difference  $V_{Xi}$  of an analog one by one over each horizontal scanning period, and a latch circuit maintains each video-signal electrical potential difference  $V_{Xi}$  over a 1 horizontal-scanning period.

[0022] In detail furthermore, DAC73 An electrical potential difference  $V_{ref1}$ , the gradation electrical-potential-difference generation section 74 by which serial arrangement of two or more resistance which corresponds to the number of gradation between  $V_{ref(s)2}$  was carried out, and the gradation electrical potential difference which corresponds based on inputted digital image data DAT A are made into the video-signal electrical potential difference  $V_{Xi}$ . The gradation voltage selection section 75 to choose and when abnormalities arise to the reference clock signal CK further corresponding to a control signal CONT1, it has the switching devices 76a and 76b of the pair which switches each of electrical potential differences  $V_{ref1}$  and  $V_{ref2}$  to the counterelectrode electrical potential difference  $V_{com}$ .

[0023] Next, the scanning-line drive circuit 81 is explained with reference to drawing 2. This scanning-line drive circuit 81 receives the perpendicular clock signal CPV and the perpendicular start signal STV from the liquid crystal controller 51, and a shift register 82 carries out the sequential transfer output of the perpendicular start signal STV based on the perpendicular clock signal CPV. This shift register 82 output is outputted through a buffer 83. Moreover, the output of a buffer 83 is connected to each scanning line Yj through the switching device 84, respectively, and if the 2nd control signal CONT2 is maintained high-level, the above-mentioned switching device 84 will choose the electrical potential difference Vgon corresponding to the high level of the scan pulse VYj.

[0024] Next, actuation of the liquid crystal display 1 mentioned above is explained below. First, when reception of the reference clock signal CK from the PC side stops according to the power source OFF or abnormality situation of a body, even if it is in the middle of operation, the liquid crystal controller 51 detects this and outputs the 1st and 2nd control signals CONT1 and CONT2.

[0025] Based on this 1st control signal CONT1, the switching devices 76a and 76b of a pair switch each of electrical potential differences Vref1 and Vref2 which is inputted into DAC73 of the signal-line drive circuit 71 to the counterelectrode electrical potential difference Vcom. Thereby, no matter image data DAT A inputted into the signal-line drive circuit 71 may be what signal, the counterelectrode electrical potential difference Vcom is outputted to each signal line Xi from the signal-line drive circuit 71.

[0026] Moreover, based on the 1st control signal CONT1, a switching device 84 chooses the electrical potential difference Vgon corresponding to the high level of the scan pulse VYj for the output of all the scanning lines Yj, and TFT21 connected to all the scanning lines Yj by this is set as switch-on.

[0027] Therefore, the counterelectrode electrical potential difference Vcom is written in all the pixel electrodes 25, the potential difference between the pixel electrode 25 and a counterelectrode 43 serves as zero, and direct current voltage is not impressed to a liquid crystal layer.

[0028] And after predetermined period progress, based on the control signal CONT3 outputted from the liquid crystal controller 51, the output of the various electrical potential differences from the electrical-potential-difference conversion means 61 is forbidden, and actuation is completed.

[0029] According to the liquid crystal display 1 of this example, as explained above, even if it is any at the time of normal or abnormal termination, it is prevented that direct current voltage is impressed to a liquid crystal layer, and, thereby, it becomes securable [ good display grace ] over a long period of time.

[0030] any of the output from the gradation electrical-potential-difference generation section 74 by which serial arrangement of two or more resistance was carried out no matter what data might be inputted into the signal-line drive circuit at the time of malfunction detection, as especially described above — although — since it becomes the counterelectrode electrical potential difference Vcom, the counterelectrode electrical potential difference Vcom is outputted to a signal line. And if constituted in this way, it is not necessary to ask a counterelectrode drive circuit for the voltage output according to individual, and circuitry can be simplified.

[0031] Although the reference clock signal CK inputted shall be supervised and termination of abnormalities of operation or actuation shall be recognized in this example, other input signals may be supervised. Moreover, the signal outputted from a liquid crystal controller by the effect of the noise from the outside etc. may become unusual. For this reason, you may constitute so that the signal outputted from liquid crystal controllers which are easy to be influenced of an external noise, such as the level clock signal CPH, may be supervised.

[0032] Although the drive circuit has been arranged out of an array substrate, in the above-mentioned example, it can also form in one on an array substrate by using the polycrystalline silicon film or the single-crystal-silicon film as a semi-conductor layer.

[0033] Moreover, as a liquid crystal layer, it cannot be overemphasized that various liquid crystal ingredients other than a TN liquid crystal, such as a ferroelectric liquid crystal and guest host

liquid crystal, are usable. Moreover, you may be the display which forms the counterelectrode which counters a pixel electrode and this superficially on an array substrate, and performs a display action using longitudinal direction electric field inter-electrode [ these ].

[0034]

[Effect of the Invention] According to the active-matrix mold display of this invention, it is prevented that direct current voltage is impressed to a liquid crystal layer over a long period of time, degradation of a liquid crystal layer can be mitigated by this, and it becomes securable [ good display grace ] for a long period of time.

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[Translation done.]